**AI’s Small Step, IC Productivity’s New Heights**

In the IC design and development process, the verification part plays a vital role. It is the main line of defense to ensure that the IC is successfully launched on the market. The task of IC verification (Verification) runs throughout the entire design process, and its core goal is to ensure that the IC design strictly meets predetermined specifications and performance requirements.

Since this year, competition in the field of artificial intelligence (AI) has become the focus of the industry. Large models represented by ChatGPT have become the "darlings" of the times, and recently, Google suddenly released the Gemini large model. The rapid development of AI technology has far exceeded our imagination. As the godfather of artificial intelligence, Geoffrey Hinton, said, “Humanity is at a turning point in artificial intelligence.”

The rapid development of AI is inseparable from the support of powerful underlying IC technology, and AI technology itself is also feeding back the IC industry. The integration of AI is also penetrating into the electronic design automation (EDA) field. In fact, in many aspects such as IC design, verification and testing, the remarkable results of AI+EDA cannot be ignored. As an early adopter of AI in the EDA and IP fields, Synopsys is using this powerful "assistant" to change the traditional verification and debugging model and improve the efficiency and productivity of IC development.

**Verification: the "Goalkeeper" for the Successful Launch of ICs**

But you may not know that IC verification engineers spend one-third of their time fixing the IC design during the entire verification process, which is called debugging. Debugging in the design stage mainly detects the IC design logic to ensure that the IC functions correctly. Today, in order to meet the needs of many applications with demanding performance requirements, ICs have become larger and more complex. “A rising tide lifts all boats,” and the debugging time and effort engineers spend to ensure it operates as expected increases exponentially.

The process of IC debugging is not only affected by size, but also by functionality and end-use purpose. For example, we often need to simulate thousands of simultaneous complex operations to test specific conditions. In this case, to find out where the problem lies, you have to do a parallel check to find the offending branch. For different end applications, special attention needs to be paid to certain signals in the design.

Therefore, a good debugging solution requires understanding all aspects of the design, such as RTL (register transfer level) and gate-level design, in order to accurately find the problem. In some cases, it is best to be able to see the hardware and software interactions at the same time so that debugging can be more effective.

However, the most troublesome thing for engineers when debugging ICs is that it requires a lot of manual operations. Because if you want to debug current complex systems, such as Multi-Die, IClet , etc., you often need to run thousands of simulations and tests to verify the design, which will generate a large amount of data. And this data usually needs to be manually sorted to find out and determine whether it is a problem with the design itself or the test platform. To run these simulations and generate reports, many teams rely on internally developed scripts that are often difficult to extend or reuse.

In addition, there are many manual operations required, such as viewing classified reports and log files, deciding where to start inspecting signal waveforms, and backtracking circuits. These manual operations rely heavily on experience, are not easily scalable, and are not conducive to improving work efficiency. Although some techniques, such as batch -mode linting, can help teams avoid some errors, it is almost impossible to achieve complete error-free design from the beginning.

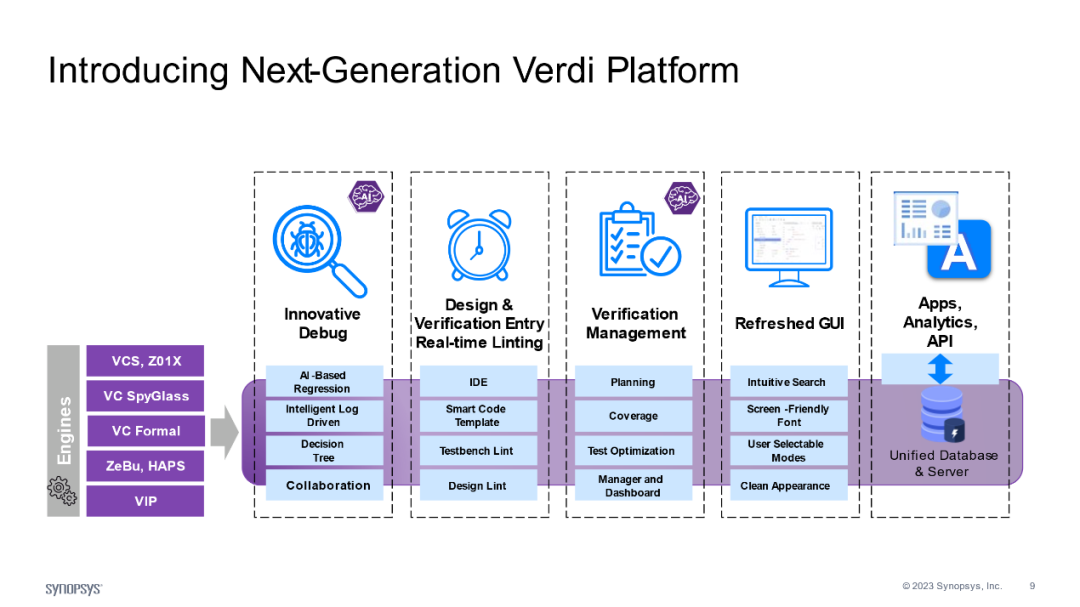
It can be seen that IC debugging is an arduous and time-consuming task in the IC verification process. Therefore, improving the efficiency of IC debugging is a top priority.

For a long time, EDA tools have played a core role in this process. If AI technology is used to improve efficiency to a higher level, it will undoubtedly be the "icing on the cake".

**Synopsys Verdi Platform: AI-driven, Accurate in Debugging and Verification**

To effectively address the growing debugging challenges and improve the overall productivity of the verification process, Synopsys leverages AI to launch the next-generation Synopsys Verdi platform , which is efficient and has comprehensive debugging and verification . This is another major step forward in the combination of AI and EDA to help engineers achieve one-time successful IC design.

The Verdi platform provides a new graphical user interface (GUI), AI-driven debugging technology, and integration with Synopsys VC Execution Manager verification management system (VMS) and Synopsys Euclide Integrated Development Environment (IDE). The entire system can view results via the Verdi platform or a web browser on a secure network. Dynamically generated and extensible decision trees support the creation and sharing of knowledge bases to promote higher debugging efficiency.



**Synopsys Verdi Platform**

In the Verdi platform, the main goals of these components are:

**1. To Prevent Primary Mistakes**

By integrating the IDE, the platform extends the scope of debugging to include not only design-under-test (DUT) but also the creation of test benches. This is achieved by providing on-the-fly code linting and synchronization with the database.

**2. To Run Regression Tests Efficiently**

The results of regression testing drive debugging, and additional testing is often required to enhance debugging. Regression testing is the responsibility of the verification management system, including planning, running or executing regression tests, and collecting and organizing test results for subsequent debugging.

**3. Using AI To Classify Errors**

The results of regression testing, usually in the form of log files, need to be categorized and their source determined (such as a problem with the DUT or the testbench), and then the errors ranked according to likelihood for priority inspection. The AI technology in the platform plays a key role in this process.

**4. Use AI To Perform Root Cause Analysis (RCA)**

After classifying errors, the next step is to determine the root causes of those errors. The AI-based RCA engine comes into play here and can help locate issues faster. 5) Share with team members. After several automation steps, interactive debugging can be performed. Additionally, results and debugging decisions can be shared globally via the server.

In addition, the Verdi platform can:

**View simulation run results** to identify which tests passed or failed, and determine whether errors occurred in the design itself or in the testbench.

**Observe code changes** and provide an assessment, as bugs often appear in waves or in cycles under specific conditions. The platform’s decision tree functionality facilitates the identification of correlation errors, paving the way for root cause analysis.

Once you've determined where the error occurred, quickly backtrack and step through the circuit to figure out what's causing the unusual behavior. This improves productivity (especially by reducing the time needed to find errors) and the quality of your results (by increasing the accuracy of error detection).

MediaTek commented: “The next-generation Synopsys Verdi platform features AI-driven regression debugging automation capabilities that can significantly help engineers reduce root cause analysis time for regression failures from days to minutes. "

Synopsys ' EDA Group , also said: "By adopting more innovative artificial intelligence technologies, we are developing Synopsys Verdi into a unified debugging and verification management system that can provide multi-site teams with scalable and will significantly reduce commissioning turnaround time for customers.

**Summary**

The integration of AI technology and EDA tools has brought great changes to IC design. This integration not only improves design efficiency and accuracy, but also opens up new design possibilities. For example, Synopsys' next-generation Verdi platform, described in this article , can help project teams achieve higher levels of productivity and greater accuracy in error detection and root cause analysis. Looking to the future, the combination of AI and EDA will continue to drive innovation in IC design. For engineers, mastering AI technology will become a necessary skill.